Experimental Validation Methods for Thermal Models

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EXPERIMENTAL VALIDATION METHODS FOR THERMAL MODELS

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Abstract

The present paper evaluates the most important experimental thermal characterisation techniques for electronic components. Weak points are indicated in the standardised methods for the still air, cold plate and fluid bath environment. Improvements have been developed: Suitable measures determine well-controlled surface temperature profiles over the whole component surface in the double cold plate. Two impinging jets impose reproducible heat transfer coefficients in the fluid bath method. Hence, the reproducibility, the scope and the accuracy of the measurements are enhanced.

1 Introduction

1.1 Thermal Modelling

Due to the impact of ever progressing integration and speed in electronic systems, which is not completely offset by the reduction in power dissipation per function, the heat load per unit area or volume continues to grow, reaching critical values in many application areas. This has brought thermal problems from an afterthought to an early system design issue.

Consequently, recent years have seen a sharp rise in the use of enclosure-level and PCB-level thermal analysis software. Enhanced computer power allows calculation of local air temperatures and heat transfer coefficients. If the analysis packages are supplied with good thermal models of the components then it becomes possible to calculate the junction temperature with sufficient accuracy to serve as an input for later reliability analyses. The PCB-level thermal analysis packages all contain thermal models of components, of varying degrees of sophistication, ranging from a single thermal resistor using the manufacturers value of R_{jc} through to quite complex thermal

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resistor networks. However, the accurate prediction of the temperature of critical electronic parts is still seriously hampered by the lack of standardized, reliable, input data: two different networks for the same part cannot be expected to produce the same results. The conclusion is that both enclosure- and PCB-level analysis require correct thermal models from a component database, according to an internationally-agreed format.

This paper discusses model validation as part of a structured approach to develop libraries of models for thermal simulation. It is based on work done in DELPHI, a CEC-sponsored project under the ESPRIT III Programme. For further details, we refer to [1]. Empirical results, specific simulations and some general project results are used to compare and enhance existing measurement methods. An actual systematic comparison between the simulations and the experiments is presented in [2].

1.2 DELPHI

The project title DELPHI stands for DEvelopment of Libraries of PHysical models for an Integrated design environment. It was proposed to create and validate generic thermal models of electronic parts. Thermal analysis is considered at all packaging levels by providing at least 2 different levels of accuracy:

- detailed models which represent sufficient physical features to permit accurate calculations of the temperature distribution throughout the package, either finite-element or finite-difference conduction models; and
- compact models for use as an approximate simplified representation (typically resistor networks modelling the heat flow paths inside).

The package itself should be modelled, nothing else. In general, one cannot assume that the component manufacturer, who eventually should supply the models [1], knows the environment to which his part will be exposed. Therefore, his responsibility should be restricted to supplying a model of the package valid for all practical environments, whereas the equipment around it is system-level engineering responsibility.

Standard R_{ja} methods, as well as useful enhancements, where R_{ja} is complemented by supplementary info (such as the sensitivity of T_j to T_{brd}, Andrews, Mahalingam, [3], [4], [5]) do not comply with this requirement. To respect this principle, a methodology has been defined, at least suitable for mono-chip packages. The 208-pin plastic quad flat pack (PQFP208) served as pilot device. As reported in [1] and [6], its compact model achieves an accuracy of 1% over 38 "practical" boundary conditions.

Clearly, one of the important objectives of the DELPHI project is to define a thermal characterization philosophy which is essentially independent of all practical boundary conditions, in other words, one which really provides a universal thermal model of the package. Accordingly, this paper describes experiments which focus on the validation of thermal conduction models for the package alone. The experiments must provide boundary conditions to be applied in simulations. This imposes more requirements then a performance comparison test, such as described in [7].

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1.3 Thermal resistance concept

Thermal characterization is typically based on some R_{th} -concept, defined as :

$$R_{th} = (T - T_{ref})/P \quad (1)$$

where P is usually the steady-state dissipation of the component, T is some critical temperature (generally the junction temperature) and T_{ref} some reference temperature, either of the case or the ambient air temperature, for which the corresponding thermal resistances are customarily denoted by R_{jc} and R_{ja}, respectively.

The definition of thermal resistance requires a greater degree of generality and care than its electrical analogue, because physical surfaces, such as the component case, are rarely isothermal and, even if they are by design, it is difficult to create a controlled region between them without heat losses to the outside world.

1.4 Device under test (DUT)

This study is based on a thermal test die (SGS-Thomson P655) packaged in a 208-pin plastic quad flat pack (PQFP208). Other test dice are also possible and are being used within the project. They all allow to spread the dissipation equally over the die and feature at least 1 centrally located temperature measurement diode.

Because of the high thermal conductivity of silicon compared to that of plastic and to a lesser extent ceramic, the variation of temperature over the silicon is often (but not always) small compared to the variation from the silicon to the case. The assumption of an isothermal silicon surface is then a good approximation. So, ideally, we have to devise an isothermal reference surface and some control of the heat fluxes.

Theoretically, the use of test boards for mechanical and electrical connection of the packages is undesirable: Acting as heat sinks they introduce additional uncertainties and distort the thermal characterization. However, as all fine pitch SMT components (0.5mm pitch), our DUT has very fragile leads. In this case, test boards are inevitable, and the parasitic effects must be minimized by special designs.

1.5 Calibration

During the calibration, the electrical values of the temperature sensitive parameter (TSP) are determined as a function of the temperature. In our case, the TSP is a forward diode voltage at a constant diode current. The acceptable calibration current range was established to be between 10μA and 1mA for our DUT. Below this range, the temperature sensitivity of the forward diode voltage tends to increase. Both 4- and 2-point measurements result in a linear calibration curve. When using 2-point calibrations however, one must always do the measurement and the calibration exactly the same way, with the same DUT, to keep the series resistance identical. Even small processing variations can generate on-chip resistance differences.

In principle the calibration is not much more than a measurement without power applied. But, since any error generated in it is introduced in all following results, we

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must pay special attention. An accurate temperature measurement is needed, other than the TSP. Typically, the same sensor as used to monitor the environment provides this value. The advantage is that a constant systematic error in the reference temperature value is cancelled out when considering temperature differences.

2 Model validation requirements

In general, test methods for validation of a thermal model should satisfy the following 6 criteria (listed more or less in order of importance):

1. They must provide well-defined boundary conditions, easy to simulate numerically: convective effects must be eliminated, because the heat transfer coefficient (HTC) is not known accurately enough.
2. They must provide all possible boundary conditions, necessary for a real validation: this means that all the boundary conditions applicable to a component at any one time must be simulated. In other words, they must be able to address all practically important heat flow paths individually or in combinations allowing mathematical extraction of those paths' separate characteristics.

The relevance of this requirement is illustrated by the "Expanded R_{jc} Methodology" (Bar-Cohen et al. [8], [9], [10]), where the analysis is also restricted to the package itself. It is characterized by a limited number of well-chosen thermal resistances in a star topology, where the centre corresponds to the junction, e.g. by placing nodes on all surfaces that take part in the heat transfer, and additionally at some lead groups.

Unfortunately, despite the fact that the Bar-Cohen method generates remarkably accurate results for a range of boundary conditions uniformly applied to all faces, such as occur in practice when testing the package in a fluid bath or (without a PCB) in still air, it failed to predict the junction temperature for other boundary conditions of interest, such as for forced convection and heat sinks. This is due to the fact that the model validation and parameter estimation are based on (numerical) experiments which don't represent all the boundary conditions adequately.

The boundary conditions can be characterized by the HTC applied to different exposed parts of the component: top, bottom, sides and leads. In [6] 38 HTC combinations are used in as many numerical experiments to develop the compact model. They represent practical component environments, in which the compact model must fit the reality. For an empirical approach, it is impractical to impose 38 different experiments for each device. Therefore we need to reduce the number of tests to a representative set, which includes the extreme (i.e. difficult for the model) conditions.

3. The tests must be reproducible: results should not be too sensitive to the details of the test implementation, and must certainly remain the same when replicated after removal of the device under test (DUT). If this is not the case it is impossible to repeat tests in different laboratories.

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The following quote from SEMI G43-87 (Fluid bath measurements of moulded plastic packages) shows this is not trivial : "... Due to the thermophysical properties of the heat transfer fluids used and the effects of the variable nature of the fluid-stirring and package-mounting procedures, this test should only be used for comparing the thermal characteristics of plastic packages in the same fluid bath system. ...".

The next 3 requirements, although not of the same scientific nature, are equally relevant if we are to obtain a widely used specification, suitable for standardization.

4. The test set-ups must be cost-effective to build and run: they must be easy to use, automation must be possible and measurements should not take too long.
5. The methods must be flexible : adaptation to a new device (type) should be easy.
6. They must be readily explicable and understandable, allowing efficient numerical simulation (without irrelevant features).
7. They must provide accurate calibration possibilities.

3 Measurement methodologies

The following approaches, based on existing and emerging standards are considered.

1. Well stirred fluid bath (FB, Semiconductor Equipment and Materials International - SEMI Standard G30-88, G43-87) to mimic the isothermal case.
2. Temperature controlled cold plate (CP, SEMI G30-88): unidirectional heat flow.
3. Still air (SA, SEMI G38-87, JC15.1)

Clearly, different methods generate different values for R_{ja} for the same package. For one specific PQFP208, FB measurements in different laboratories showed values between 7.4 and 18.5K/W. CP results on the same component ranged between 8.3 and 12.1K/W and SA results between 34.5 and 38.5K/W. For R_{jc}, a totally different picture was obtained: 4.4K/W for SA, 7.2K/W for FB and 11.3K/W for CP. Of course, the latter results only have a very limited, relative, value since the case is not isothermal, as explained earlier, and T_c measurements are unreliable in general.

3.1 Fluid bath (FB)

The simplest possible surface temperature distribution is the isothermal one but it is difficult to contrive experimentally. It requires very high HTCs : the temperature drop across the region between isothermal ambient (bulk fluid) and component case must be negligible. The necessary HTC depends on the DUT. For an isothermal case, the HTC needed to reduce the R_{ca} to a certain fraction of R_{jc} is calculated in table 1. An outer area of $2.10^{-3}\,m^2$ is assumed, typical for a PQFP208, or a PGA.

This is the intention of the fluid bath, in which the part is suspended in an agitated fluid: the high specific heat of the fluid coupled with the agitation will lead to a very high heat transfer coefficient at all points of the case. If the target from table 1, last column is not met, the HTC must be known and reproducible. In this case, the set-up has to be specified in full detail (bath dimensions, test board and clamps, stir-

Table 1 : HTC required to reduce R_{ca} to a certain fraction of R_{jc}

R_{jc} (K/W)	HTC (W/m²K) required to make	
	$R_{ca} = R_{jc}$	$R_{ca} = 0.01\ R_{jc}$
10	50	5000
5 (PQFP)	100	10000
1 (PPQFP)	500	50000

rer/pump type, rate and pipes), which is highly undesirable (not flexible, not robust), or a set-up has to be devised which forces the fluid flow, independent of the DUT.

The two fluids mostly used in a fluid bath, are fluorinert and de-ionized water. Fluorinert is often preferred because it is electrically insulating by nature. However, a thermally better choice is de-ionized (DI) water, which has a 4 times bigger specific heat. Furthermore, the viscosity of fluorinert depends on temperature, resulting in different thermal resistances at different fluid temperatures (powers). Unfortunately, DI water is more difficult to handle (to keep it DI to avoid leakage currents and corrosion). The SEMI standard does not define the kind of fluid to be used nor the degree of agitation.

Measurements were performed in a fluid bath for a range of dissipations with those two fluids, in both natural convection and forced convection, the latter using stirring and recirculation pumps. All these tests turned out to be hard to interpret (HTC unknown) at best, and mostly not even reproducible between different laboratories. More details can be found in [11]. The main problems were due to the influence of the DUT on the flow, with usually a very unsteady flow, and a HTC that wasn't high enough, so there was also significant dependence on the fluid stirring rate.

In [11], the enhancements from the standard fluid bath to the submerged double jet impingement test (SDJI) are described. The use of 2 impinging fluid jets offers the highest HTCs and solves the other mentioned FB problems. When the bath is suffi-

Table 2 : Heat transfer coefficients for fluidum-based methods

Application		P (W)	T_{wall} (°C)	HTC (W/m²K)	Remark
SA	Nat. conv.	1-5	40-100	12-15	
FB, natural convection	FC-70	5-10-20	34-42-54	96-119-150	
	DI water	5-10-20	23-25-28	418-495-609	
SDJI	DI water	10-20	20.37-20.51	13800-14800	V = 10l/min
	optimized	-	-	40000	optimized jets
Tested with aluminum plates glued to heater foil, size 50mm x 50mm.					

ciently large, the outlet nozzles determine the flow and the HTC, not the bath and DUT geometry. With a flow rate of 10l/s HTCs around 40000W/m²K can be obtained. Table 2 illustrates the potential of some fluidum-based measurement methods.

For calibration, the situation is totally different: as there is no significant heat flow, all fluid bath systems provide a stable and uniform environment. No differences could be observed between fluorinert or DI water baths, [11].

3.2 Natural convection

Natural convection is one of the predominant modes of cooling. Provided the ambient is isothermal, the R_{ja}-definition can be applied straightforward, for all the heat dissipated at the junction ends up in the environment. However, R_{ja} depends strongly on the application method: very different values apply to, for example, an isolated component in still air compared with a board-mounted component with a heat sink. Therefore a very specific standard is needed to obtain reproducible results. This is achieved by the JEDEC-standard (no heat sink) and the corresponding SEMI standard (vertical test board only). The test set-up is very cheap and flexible, since the main contributors to hardware and cost are also needed in every other method.

The main disadvantage of the method is its insensitivity to the actual device conduction model: When splitting R_{ja} into two components, the conduction resistance R_{jc} and the resistance from case to ambient R_{ca}, the latter will typically predominate (since the package is not isothermal, the meaning of both resistances is not precisely defined). This term is mainly determined by the environment: convection, conduction in the test board and radiation. R_{ja} varies between 35 and 38K/W for the PQFP. Clearly, conduction is only responsible for less than 30% of this. In [13], the still-air measurement is simulated : 75% of the generated heat entered the test board trough the leads (and is then convected), about 10% was radiated and about 10% was directly convected in the air. Still-air measurements only characterize the complete assembly, component and board. In [13] it is only applied to the detailed model, and is complemented by infra-red thermography, to map the case temperature contours.

3.3 Cold plate

The purpose of the cold plate method is to extract all the heat through the copper or aluminum cold plate. The cold plate should force the component case to a known constant temperature, which defines R_{jcp}. The 2 main issues associated with the cold plate are heat losses and interface resistances.

Interface resistances can add a major term in R_{jcp}, as shown by Kozarek in [12] and move the isothermal surface away from the component. The effect of a layer of air (k = 0.0261W/mK),0.050mm thick, is detrimental : assuming 1-dimensional heat flow it adds 2.5K/W. To reduce their effect, it is imperative to use some kind of adhesive and apply pressure on the device. The same layer, now with k = 2W/mK has a more than 80 times lower thermal resistance, which falls well within the manufac-

turing tolerances, [2]. We have used uncured thermally conductive adhesive, thermal paste and Indium foils. No significant difference was found. Also when comparing enhanced cold plate tests (DCP-1, see further) with SDJI tests, only minor differences were found. At least for the PQFP, interface resistances can be neglected when using good quality interface material and a well-built cold plate clamp, see [2]. We also tried to measure the case temperature directly, in stead of the temperature of the copper block below it, but found this not accurate and not reproducible. As demonstrated in [12] for a ceramic PGA, the thermocouple size is critical : unless a surface thermocouple is used one may read some temperature in the adhesive. For plastic packages, the situation is worse because the thermocouple itself will evacuate some heat, locally reducing the plastic temperature.

Heat losses could be minimized in 2 ways : insulating the component thermally and creating an ambient at the junction temperature. Certainly the latter cannot be done perfectly, as the test is based on a temperature difference. As there is no perfect insulator (lowest practical conductivities: 0.2-0.02W/mK), we must accept some heat losses. This is not covered in G30-88, the SEMI standard for ceramic packages, which specifies neither the insulation, nor boundaries for the cold plate environment.

The cold plate temperature varies typically between 60ºC (a hot PCB), and 20ºC. For materials with significantly variable conductivity, the first environment is the most relevant one, as it represents the worst case. Low cold plate temperatures could be chosen to lower the junction temperature to the ambient, so as to maximize the heat flow in the cold plate. A T_{cp} around, or below 0ºC will be needed, resulting in condensation, and even freezing of the coolant, which makes this setting very impractical.

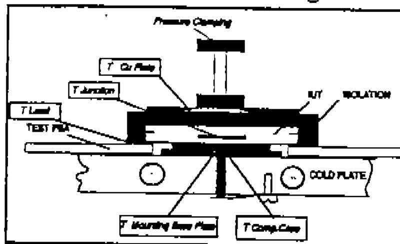

Figure 1 : Single cold plate fixture

Where power losses away from the (isothermal) cold plate cannot be avoided (i.e. the boundary is not adiabatic), we must provide for another temperature-controlled boundary completing the DUT enclosure. So the cold plate environment must be adapted to provide a well-known temperature distribution on the full surface. Although, in theory, an IR scan of this area should suffice [12], comparison with simulation becomes cumbersome. A copper or aluminum box, dimensioned to be isothermal, around the insulator is characterized by just 1 temperature. Our PQFP208 only needs a top plate, as the sides have a negligible influence. Simulations have shown a sensitivity of T_j to the top boundary temperature T_t of 16% (for P= 2, 6W and T_{cp}= 40, 60ºC) to 20% (for P= 1W and T_{cp} = 20, 40, 60ºC) : a lowering of 10ºC in T_t results in a lowering of 1.6 to 2ºC in T_j. This is quite acceptable for performance comparisons. For validation purposes, i.e. in combination with a simulation model, the added accuracy from a completely characterized outer boundary is essential. In the following figures such a top cover is always assumed.

Figure 2 shows the power leaving the cold plate in function of the cold plate temperature, and figure 3 the corresponding temperature difference (which would be the thermal resistance if the ambient were isothermal). Both graphs were obtained by simulation. The PQFP (3.6mm thick) sits in an insulator block of 5mm height, with a thermal conductivity of 0.15W/mK, and dissipates 1W. The insulator material is covered by the copper plate. Normally, this plate is freely cooled in the air, with natural convection in a 20ºC ambient (HTC= 15W/m²K). The fraction of power entering the cold plate decreases with increasing T_{cp}, and so does ΔT_{cp}.

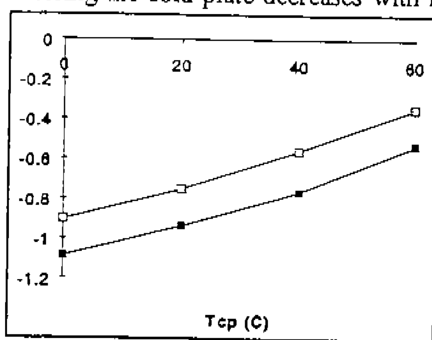

Figure 2 : Cold plate power
■ : top cold plate free, HTC=15W/m²K - □ : top fixed at app. 5ºC below its simulated value

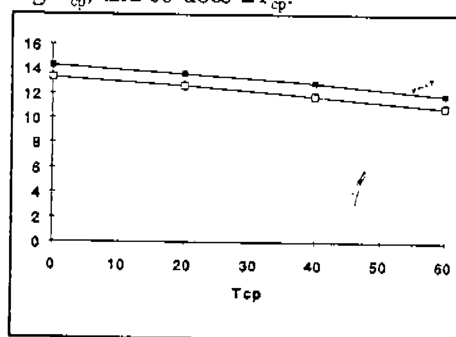

Figure 3 : ΔTjcp in function of Tcp
■ : top cold plate free, HTC=15W/m²K - □ : top fixed at app. 5ºC below its simulated value

For calibration, the interface resistances are not relevant, but heat losses are. If the (local) ambient is not fully raised to the cold plate temperature, a temperature gradient develops across the component, resulting in differences between T_j and T_{cp}.

3.4 Double cold plate (DCP)

An obvious extension from the isothermal insulator casing is to equip it with a temperature control device. The device under test is sandwiched between two cold plates with a spacer between the package top and the upper cold plate, as illustrated in figure 4. Analysis with FLOTHERM reveals that a low conductivity spacer results in a temperature distribution on the top of the package akin to what is found there in natural convection conditions. Alterations of spacer conductivity alter the path of heat escape from the package with more or less leaving via top, bottom or leads. Nothing changes with respect to the interface resistances. There are 3 alternatives for the top.

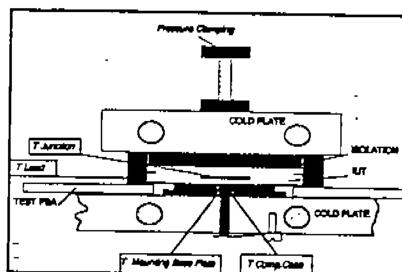

Figure 4 : Double cold plate fixture

1. The top cold plate is floating and acts as a more or less efficient heat sink in air. It can be modelled as a fixed iso-thermal boundary because it provides a uniform surface temperature, although it is not enforced actively.

Figure 5 shows simulated temperature differences between junction and cold plate for our DUT, dissipating 1W, and with a 3mm spacer (k=0.15W/mK), as compared to the 1.4mm in previous graphs. The HTC at the top area is assumed 15W/m²K. Figure 6 shows the bottom cold plate power.

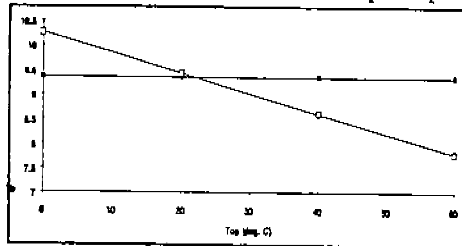

Figure 5: Double cold plate: ΔT_{jcp} (K)
□: top cold plate free, HTC=15W/m²K
■: top fixed at bottom temperature

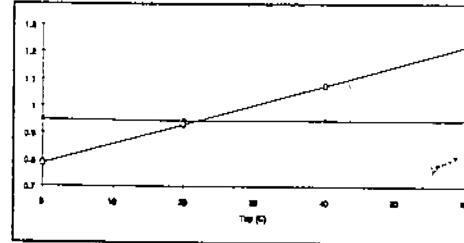

Figure 6 : DCP - plate power, P_{cp}
□: top cold plate free, HTC=15W/sqmK
■: top temperature same as bottom.

2. Both cold plates are at the same reference temperature. Then it is possible to use only 1 cooling system with the same coolant. Of course, both plates are monitored independently. The difference in heat flow is caused by inserting an insulator between the component and the top cold plate. Practical spacer materials have thermal conductivities of 0.2-0.02W/mK for an insulator and 200-400 W/mK for metals (Cu or Al).

Those tests are illustrated in figures 5 and 6, curves "fixed top". They show that this mode of operation ensures independence from the reference temperature for the most important physical quantities involved in the test. Furthermore, it guaranties that there is really only 1 reference temperature, as required in equation (1). Validation consists then in comparing always 1 thermal resistance value (junction to isothermal ambient) between measurement and simulation. For the low HTC, with insulating spacer, test results are fairly insensitive to its thickness and conductivity [2]. Also the cold plate calibration accuracy improves, as the environment is quasi iso-thermal.

3. The last mode of operation of the dual cold plate system is with two cold plates independently controlled. The investment is higher in this case: typically the most expensive part of the set-up is the temperature control equipment. If the validations call not only for a difference in heat flow but also for a highly non-isothermal top surface, we still have to insert a thermally insulating spacer.

Clearly, the last approach yields no additional advantage for a linear system (thermal conductivity constant). Hence we prefer alternative 2. A test sequence was defined that seems to validate all important features of the PQFP, [2]:

DCP-1: No spacers, thermal interface resistances minimized. This test resembles SDJI.

DCP-2: Insulating spacer on top, 5mm thick. This test mimics use of a heat sink.

DCP-3: Insulating spacer on bottom (same as 2, but with component flipped upside down, i.e. top heat sink).

DCP-4: Insulating spacer on top, thin insulator on bottom, between leads (air). Good thermal contact between leads and cold plate. This test represents component

Table 3 : Heat transfer coefficients in the tests

Application		HTC_{TOP} (W/m^2K)	HTC_{BOT} (W/m^2K)	HTC_{SIDE} (W/m^2K)	HTC_{LEAD} (W/m^2K)
SDJI		>10000	>10000	500	500
Double Cold Plate	DCP-1	10000	10000	40	40
	DCP-2	40	10000	40	40
	DCP-3	10000	40	40	40
	DCP-4	40	40	40	10000
Still air		30 - 10 (22.5)	30 - 10	30 - 10	10 - 30

Under the assumption of a 5mm thick isolator with 0.2W/mK thermal conductivity (canvas)

mounting without heat sink, but with an important thermal path to the board. Table 3 lists the HTC combinations that are realized experimentally.

4 Conclusions

The single cold plate is not an accurate calibration environment. All others are, but the oven typically requires more than 6 times longer settling times than the rest of them. The settling times for FB (SDJI) and DCP are determined by the cooling aggregate : high capacity systems need more time.

The DCP with both plates at the same temperature promises the best overall performance. A range of well-defined boundary conditions for verification of the corresponding conduction-only simulations is available. SDJI avoids the interface

Table 4 : Test method performance summary

Test method		BC well-def.	all BC	repr.	low-cost	flex.	underst.	cal
Fluid bath	FC-70	x	-	-	-	x	-	+
	DIW	x	-	-	+	x	-	+
	SDJI	+	x	+	+	+	+	+
Cold plate	open	-	x	-	+	+	x	-
	closed	+	+	+	+	+	+	-
	DCP	+	+	+	+	+	+	+
Free air		-	-	x	+	+	-	x

resistances which may trouble cold plate measurements, but it is not trivial to realize the low HTCs in this test. The following table summarizes the performance of the investigated measurement methods with respect to the aforementioned requirements.

5 Acknowledgements

The authors acknowledge the support for this work by the Commission of the European Communities under the ESPRIT contract DELPHI (9197). They also wish to thank the other members of the project: P. Zemlianoy from Alcatel Espace, H.I. Rosten and J. Parry from Flomerics, C. Cahill from NMRC, C. Lasance from Philips CFT and T. Gautier and Y. Assouad from Thomson CSF. At IMEC a lot of work was done on fluid bath tests, especially by F. Christiaens and E. Beyne.
FLOTHERM is a registered trademark of Flomerics Limited.

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